REMARKS/ARGUMENTS

The Applicant has further amended the claims. The Applicant respectfully submits that amendments to the claim set are fully supported by the originally filed specification.

Independent claims 1, 2 and 7 have been amended to include the limiting features of original dependent claim 6.

In the second Office Action the Examiner considered claims 3 and 6 as defining allowable subject matter if rewritten in independent form. In the third Office Action, the Examiner raised newly identified prior art to reject independent claims 1, 2 and 7 after amendment to incorporate the feature defined in original claim 3. Also in the third Office Action, no rejection was raised against dependent claim 6 based on the newly identified prior art. Hence, currently amended independent claims 1, 2 and 7 now incorporating the limiting features of original claim 6 are allowable.

In relation to the 35 USC §112 rejection, the Applicant respectfully points out a fundamental inconsistency in the Examiner's rejections. Under the 35 USC §103 rejection, the Examiner states: "Official Notice is taken that it is well known in the art of microcontrollers and processors to utilize a wafer substrate to position the processor circuitry". In the present claims the microcontroller includes processor circuitry, print head interface circuitry and bus interface circuitry. The Examiner relies on an argument that it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the elements of the microcontroller on a wafer substrate.

In conflict to this position, under the 35 USC §112 rejection, the Examiner states: "The written description lacks adequate support for positioning the print head interface on the wafer substrate". However, 35 USC §112 requires that the written description enables any person skilled in the art to make and use the same. As the Examiner considers this feature of the claims obvious under 35 USC §103, the Examiner should not also consider that the person skilled in the art could not make and use the same.

Moreover, the Applicant highlights to the Examiner the discussion of the print head interface (beginning page 139):

"The Print Head Interface 62 connects the ACP to the Print Head, providing both data and appropriate signals to the external Print Head. The Print Head Interface 62 works in conjunction with both a VLIW processor 74 and a software algorithm running on the CPU in order to print a photo in approximately 2 seconds.

An overview of the inputs and outputs to the Print Head Interface is shown in Fig. 154. The Address and Data Buses are used by the CPU to address the various registers in the Print Head Interface. A single BitClock output line connects to all 8 segments on the print head. The 8 DataBits lines lead one to each segment, and are clocked in to the 8 segments on the print head simultaneously (on a BitClock pulse). For example, dot 0 is transferred to $segment_0$, dot 750 is transferred to $segment_1$, dot 1500 to $segment_2$ etc. simultaneously."

Only one wafer substrate is discussed in the written description by reference to a single microcontroller. Fig. 3 clearly shows a central processor 31 which includes the VLIW vector processor 74 and the print head interface 84 on the same processor 31. Still furthermore, Fig. 2 clearly illustrates a central processor 31 communicating with the print head 44, it is obvious that the print head interface of Fig. 3 is part of the central processor 31 in Fig. 2 for which it is also obvious (by the Examiner's own statements) that a single wafer could be used to construct the central processor 31.

The Examiner's reconsideration of this rejection is requested.

CONCLUSION

In view of the foregoing, it is respectfully requested that the Examiner reconsider and withdraw the rejections under 35 USC §112 and 35 USC §103. The present application is believed to be in condition for allowance. Accordingly, the Applicant respectfully requests a Notice of Allowance of all the claims presently under examination.

Very respectfully,

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